	Application No.	Applicant(s)	
Notice of Allowability	09/716,977	DUNLOP ET AL.	
	Examiner	Art Unit	
	Eva Yi Zheng	2634	
The MAILING DATE of this communication apperature All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RI of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED in this ap or other appropriate communication GHTS. This application is subject to	plication. If not include will be mailed in due o	d course. THIS
1. \square This communication is responsive to $2/7/05$.			
2. The allowed claim(s) is/are <u>1-36</u> .			
3. \boxtimes The drawings filed on $\underline{5/18/01}$ are accepted by the Examine	er.		
4.			
Attachment(s) 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal F 6. ☐ Interview Summary Paper No./Mail Da 7. ☐ Examiner's Amendr 8. ☑ Examiner's Stateme 9. ☐ Other	(PTO-413), te ment/Comment	·

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed December 2, 2004, with respect to claim 1-36 have been fully considered and are persuasive. The claim rejections have been withdrawn.

Allowable Subject Matter

- 2. Claims 1-36 are allowed.
- 3. The following is an examiner's statement of reasons for allowance:

None of the prior art teaches or suggests a clock recovery system that operates in a burst mode to recover the clock signal from an early bit in the incoming data. In specific, the system comprise a first phase-locked loop (PLL) circuit for generating an oscillator signal having substantially the same frequency as a transmitter clock and for generating a bias signal; and a second PLL circuit for generating a clock output signal, wherein the second PLL circuit is controlled by the bias signal generated by the first PLL circuit in a first mode and wherein the second PLL circuit has a second mode wherein the second PLL has an initial frequency determined by the bias signal and whereby the second PLL substantially instantaneously adjusts the clock output signal to phase changes of data in an input data stream without utilizing the bias signal.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Eva Yi Zheng whose telephone number is (571) 272-

3049. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number

for the organization where this application or proceeding is assigned is 703-879-9306.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal

Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the Technology Center 2600 Customer Service Office

whose telephone number is (703) 306-0377.

Eva Yi Zheng Examiner Art Unit 2634

April 27, 2005

Slowery line

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PRIMARY EXAMINER